



PATENT

17795 (Tyco 6)

Appl. No. 10/075,406  
Amdt. dated February 14, 2002  
Reply to Office action of April 18, 2003

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JUL 22 2003  
TECHNOLOGY CENTER 2800

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

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1 1. (original): A substrate for an area array package,  
2        said substrate having a plurality of signal wirings, each having a first contact  
3        adapted to be connected to a respective terminal of an integrated circuit, and a second  
4        contact on a periphery of the substrate,  
5        said substrate having a ground structure including, for each signal wiring, a pair of  
6        rectangular ground plane portions located on opposite sides of the second contact of  
7        that signal wiring, and  
8        said substrate having a plurality of ground via holes through the substrate,  
9        including at least one respective ground via hole through each rectangular ground plane  
10      portion.

1 2. (original): The substrate according to claim 1, wherein each ground plane portion  
2        has a plurality of ground via holes therethrough.

1 3. (original): The substrate according to claim 1, wherein for each second contact,  
2        the respective ground plane portions are connected by a third ground plane portion on a  
3        third side of the second contact.

1 4. (original): The substrate according to claim 3, wherein the third ground plane  
2        portion has a plurality of ground via holes therethrough.

1 5. (original): The substrate according to claim 3, wherein the third ground plane  
2        portions of each second contact on at least a side of the substrate are continuously  
3        connected.

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1 6. (original): The substrate according to claim 1, wherein each pair of adjacent ones  
2 of the second contacts have a single rectangular ground plane portion therebetween.

1 7. (original): The substrate according to claim 1, wherein the substrate has an  
2 opening therethrough sized and shaped to receive the integrated circuit.

1 8. (original): An area array package comprising:  
2 a substrate having:

3 a plurality of signal wirings, each having a first contact adapted to  
4 be connected to a respective terminal of an integrated circuit, and a second  
5 contact on a periphery of the substrate,

6 a ground structure including, for each signal wiring, a pair of  
7 rectangular ground plane portions located on opposite sides of the second  
8 contact of that signal wiring, and

9 a plurality of ground vias through the substrate, including at least  
10 one respective ground via hole through each rectangular ground plane  
11 portion;

12 a cover above the substrate, and

13 a bottom layer of the package formed of a dielectric material.

1 9. (original): The package of claim 8, further comprising an intermediate dielectric  
2 layer between the bottom layer and the substrate, the intermediate dielectric layer having  
3 an additional ground structure thereon.

1 10. (original): The package of claim 9, further comprising a third ground structure  
2 between the bottom layer and the intermediate layer.

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1 11. (original): The package of claim 9, wherein the additional ground structure has a  
2 ground opening around a signal via that is coupled to the second contact, the ground  
3 opening being generally shaped like a rectangle with two mitered corners.

1 12. (original): The package of claim 8, wherein the package has a signal via beneath  
2 each second contact, and a ground via beneath each ground via hole, each of the signal  
3 vias and ground vias being electrically connected to a respective solder attach pad on the  
4 bottom layer.

1 13. (original): The package of claim 12, wherein each signal via is surrounded on  
2 three sides.

1 14. (original): The package of claim 13, wherein each signal via is surrounded by at  
2 least seven ground vias.

1 15. (original): The package of claim 8, further comprising a superstrate above the  
2 substrate, the superstrate generally being formed of the same material as the substrate.

1 16. (original): The package of claim 15, wherein the superstrate has an opening  
2 therethrough above each second contact.

1 17. (original): The package of claim 16, wherein the opening above each second  
2 contact is cylindrical and is greater in diameter than the ground vias.

1 18. (original): The package of claim 16, wherein the opening above each second  
2 contact is filled with a material having a sufficiently low dielectric constant to reduce the  
3 radiation from a region of the second contact significantly.

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1 19. (original): The package of claim 8, wherein the package includes a plurality of  
2 pockets, each pocket shaped and sized to accommodate an integrated circuit.

1 20. (original): A printed circuit board assembly, comprising:  
2 a printed circuit board having a circuit board substrate with circuit traces and a  
3 plurality of devices thereon, said plurality of devices including at least one integrated  
4 circuit package assembly that includes:  
5 a package substrate having:  
6 a plurality of signal wirings, each having a first contact adapted to  
7 be connected to a respective terminal of an integrated circuit, and a second  
8 contact on a periphery of the package substrate,  
9 a ground structure including, for each signal wiring, a pair of  
10 rectangular ground plane portions located on opposite sides of the second  
11 contact of that signal wiring, and  
12 a plurality of ground vias through the package substrate, including  
13 at least one respective ground via hole through each rectangular ground  
14 plane portion;  
15 a lid above the package substrate, and  
16 a bottom layer of the package formed of a dielectric material, the bottom layer  
17 having a plurality of solder attach pads, electrically connected to contacts of the circuit  
18 board substrate.

1 21. (original): An area array package comprising:  
2 a substrate having a plurality of signal wirings, each having a first contact adapted  
3 to be connected to a respective terminal of an integrated circuit, and a second contact on a  
4 periphery of the substrate, the substrate having a signal via penetrating each second  
5 contact;

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6        a superstrate formed of a dielectric material above the substrate, the superstrate  
7        having a respective opening therethrough above each second contact;  
8        a lid above the superstrate; and  
9        a bottom layer of the package formed of a dielectric material.

1        22. (original): The package of claim 21, wherein the opening above each second  
2        contact is cylindrical and is greater in diameter than the ground vias.

1        23. (original): The package of claim 21, wherein the superstrate is formed of the same  
2        material as the substrate.

1        24. (original): The package of claim 21, wherein the substrate has a plurality of  
2        ground vias therethrough, at least partially surrounding each of the signal vias.

1        25. (original): The package of claim 24, wherein the substrate has a plurality of  
2        rectangular ground plane portions surrounding each of the signal vias on three sides, the  
3        ground vias penetrating the ground plane portions.

1        26. (Withdrawn): A method for forming an area array package comprising the steps  
2        of:  
3                forming a plurality of signal wirings on a substrate, each signal wiring having a  
4                first contact adapted to be connected to a respective terminal of an integrated circuit, and  
5                a second contact on a periphery of the substrate, the substrate being formed of a type of  
6                material suitable for use in a printed circuit board;  
7                forming on a bottom layer of the area array package a plurality of solder attach  
8                pads aligned with the plurality of second contacts;  
9                forming a plurality of signal via holes penetrating the second contacts and solder  
10          attach pads and penetrating through the substrate and the bottom layer;  
11          filling the signal via holes with a conductive liquid capable of solidifying ; and

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12 solidifying the conductive liquid to form conductive signal vias.

1 27. (Withdrawn): The method of claim 26, further comprising plating the conductive  
2 vias.

1 28. (Withdrawn): The method of claim 26, further comprising  
2 forming ground regions on the substrate;  
3 forming on the bottom layer a plurality of ground solder attach pads aligned with  
4 the plurality of ground regions;  
5 forming a plurality of ground via holes penetrating the ground regions and ground  
6 solder attach pads and penetrating through the substrate and the bottom layer;  
7 filling the ground via holes with additional conductive liquid capable of  
8 solidifying ; and  
9 solidifying the additional conductive liquid to form conductive ground vias.

1 29. (Withdrawn): The method of claim 26, wherein:  
2 the substrate is formed of a material comprising PTFE with a ceramic filler, and  
3 the bottom layer is formed of a glass reinforced hydrocarbon/ceramic laminate.

1 30. (Withdrawn): The method of claim 29, further comprising attaching a superstrate  
2 above the substrate, the superstrate generally being formed of the same material as the  
3 substrate.

1 31. (Withdrawn): The method of claim 29, further comprising attaching a lid above  
2 the substrate, the lid being formed of FR4 or similar epoxy glass laminate.

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